IN THE CLAIMS

1. (Currently amended) A coarse delay tuner circuit for use with delay locked loops, said coarse delay tuner circuit comprising: an input node for receiving an input signal, wherein said input signal is a clock signal; a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit ~~is adapted to~~ conditions said input signal and to provides a first output signal in response to a threshold level being reached by said input signal; an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit ~~is adapted to~~ receives said first output signal, said edge suppressor circuit ~~adapted to~~ providinge a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal; and an output node for outputting said third output signal.

2. (Currently amended) The coarse delay tuner circuit of claim 1, further comprising a signal conditioning circuit operationally connected to said input node, said signal conditioning circuit ~~adapted to~~ preparinge said input signal for use by said triggering circuit.

3. (Original) The coarse delay tuner circuit of claim 2, wherein said signal conditioning circuit is a low pass filter circuit.

4. (Original) The coarse delay tuner circuit of claim 3, wherein said low pass filter circuit is a first order R-C network.

5. (Original) The coarse delay tuner circuit of claim 1, wherein said triggering circuit is a Schmitt trigger circuit.

6. (Original) The coarse delay tuner circuit of claim 1, wherein said edge suppressor circuit further comprises: a first D-flipflop, said first D-flipflop having a clock input

connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate; an inverter connected to said first output signal for producing an inverted input signal; a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flip-flop; said first NAND gate having an output connected to a second input of a second NAND gate; and said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for providing said third output signal.

7. (Original) The coarse delay tuner circuit of claim 1, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period relative to the clock signal.

8. (Currently amended) A method for reducing lock time in a delay locked loop (DLL), said method comprising: providing an input node for receiving an input signal, wherein said input signal is a clock signal; providing a triggering circuit, said triggering circuit operationally coupled to said input node, wherein said triggering circuit ~~is adapted to~~ conditions said input signal and ~~to~~ provides a first output signal in response to a threshold level being reached by said input signal; providing an edge suppressor circuit operationally coupled to said triggering circuit, wherein said edge suppressor circuit ~~is adapted to~~ receives said first output signal, said edge suppressor circuit ~~adapted to~~ providinge a positive step signal as a second output signal, and wherein said edge suppressor circuit includes combinational means for logically combining said first output signal and said second output signal to produce a third output signal; and providing an output node for outputting said third output signal.

9. (Currently amended) The method of claim 8, further comprising a signal conditioning circuit operationally connected to said input node, said signal conditioning circuit ~~adapted to~~ preparinge said input signal for use by said triggering circuit.

10. (Original) The method of claim 9, wherein said signal conditioning circuit is a low pass filter circuit.

11. (Original) The method of claim 10, wherein said low pass filter circuit is a first order R-C network.

12. (Original) The method of claim 8, wherein said triggering circuit is a Schmitt trigger circuit.

13. (Original) The method of claim 8, wherein said edge suppressor circuit further comprises: a first D-flipflop, said first D-flipflop having a clock input connected to said first output signal, a data input, a reset input connected to a power on reset signal, and an output connected to a first input of a first NAND gate; an inverter connected to said first output signal for producing an inverted input signal; a second D-flipflop, said second D-flipflop having a clock input connected to said inverted input signal, a data input connected to a power supply, a reset input connected to said power on reset signal, and an output connected to a second input of said first NAND gate, and to said data input of said first D-flip-flop; said first NAND gate having an output connected to a second input of a second NAND gate; and said second NAND gate having a first input connected to said first output signal, and said second NAND gate having an output for outputting said third output signal.

14. (Original) The method of claim 8, wherein said clock signal has a rising edge and a period, and said third output signal has a rising edge with a delay of about 75% of said period relative to the clock signal.

15. (Canceled)

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